SMIC MPW Shuttle Schedule

MPW Notice To serve all customers smoothly, following items must be noticed:

1. Only standard Process/Layers products can attend MPW. No bumping, No Bank and No Corner Split allowed.
2. On one shuttle, 4 seats (including sub-chip in one seat) are the maximum that one customer can get.
3. **MPW only provides 50 dies for function verification.**
4. Shuttles are subject to cancellation if there are not enough passengers on board.
5. Without completion of below items before shuttle start date, shuttle reservation will not be held!
   - **Quotation** should be ready
   - **DRC** must be clean
   - SMIC **IP merge** case must be closed (related information need to be submitted at least **3 days** before shuttle start date)
   - GDSII and tape out forms all need to be Approved by mask shop
   - **PTOS** should be approved
6. SMIC dicing size limit: 1500um < X < 12000um, 1500um < Y < 12000um.
7. For 300mm shuttle, suggest use metal scheme condition: 6(M1-M6)+TM1(9kA)+TM2(9kA)+14.5kA ALPA+12mil BG.
8. Overdue MPW booked cases will be cancelled within 90 days after shuttle start.

Tech Node	IO Voltage/Tech Type/Char	RF	2019 MPW Booking Cut-Off Date											
			Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
28nm	IO=1.8V | IO=2.5V **CMOS Logic (HP)**	Y			5 Q58 (Fab2)			18 Q5K (Fab2)			3 Q5Q (Fab2)			
40nm	IO=1.8/2.5V| IO=1.8V| IO=2.5V **CMOS Logic (LL|UP)**	Y		12 Q55 (Fab2)				4 Q5J (Fab2)			10 Q5R (Fab2)			10 Q5Z (Fab2)
	IO=8/32V **CMOS High Voltage (HV) ***													
55nm	IO=2.5/5V | IO=2.5V **Adv. Emb-Flash (Cu-BEOL) (LL|UP)**						14 Q5G (Fab2)						19 Q5X (Fab2)	
	IO=1.8/2.5V | IO=1.8V| IO=2.5V **CMOS Logic (LL|UP)**	Y		19 Q56 (Fab2)		16 Q5E (Fab2)			16 Q5M (Fab2)			22 Q5W (Fab2)		
	IO=6/32V | IO=8/32V **CMOS High Voltage (HV) ***													
0.11/0.13um	IO=3.3V **CMOS Logic (GE)|Mixed Signal (GE)**	Y	15 Q54 (Fab1)		19 Q59 (Fab1)		28 Q5H (Fab1)			6 Q5N (Fab1)		15 Q5V (Fab1)		17 Q5Y (Fab1)
0.13um	IO=3.3/5V| IO=5V **Adv. Emb-EEPROM (Cu-BEOL) (LL)**			26 Q57 (Fab1)						27 Q5P (Fab1)				
0.15um	IO=13.3V **CMOS High Voltage (HV) ***												5 Q61 (Fab1)	
0.153um	IO=3.3V **CMOS Logic (GE)|Mixed Signal (GE)**	Y			12 Q5C (Fab1)									
0.18um	IO=5/6/9/12/16/20/24/30/35/40 **BCD performance enhanced (EP) ***	Y									10 Q5T (Fab1)			
0.18um	IO=3.3V| IO=5V **CMOS Logic (GE)|Mixed Signal (GE)**	Y	8 Q53 (Fab1)		5 Q5B (Fab7)		7 Q5F (Fab1)		9 Q5L (Fab7)		3 Q5S (Fab1)		12 Q60 (Fab1)	
	IO=3.3/5V| IO=5V **EEPROM Embedded (GE)**					9 Q5D (Fab1)						8 Q5U (Fab7)		

* 2019 new offered feature: 40nm/55nm/0.15um HV & 0.18um BCD

Version: 1.0 Update Date: 2018-9-26

Note: Please login SMIC-Now to find the most updated MPW schedule. (请登录Smic-Now以查阅最新MPW Schedule.)